

Application No.: 10/826,725

Docket No.: JCLA6643-D

Amendments To Claims

1-4 (canceled)

5. (currently amended) An electrostatic discharge (ESD) protection circuit, suitable for use on the I/O pad, the ESD protection circuit comprising: a silicon controlled rectifier (SCR) circuit, which comprises a first connection terminal, a second connection terminal, and a third connection terminal, wherein the first connection terminal and the second connection terminal are respectively connected to the I/O pad and a ground voltage, so as to discharge the electrostatic charges; and an anti-latch-up circuit, which comprises a fourth connection terminal, a fifth connection terminal, and a sixth connection terminal, respectively coupled to a voltage source, the ground voltage, and the third connection terminal of the SCR circuit, whereby when a to-be-protected IC is powered by the voltage source, an anti-latch-up signal is sent from the sixth connection terminal, so that the SCR circuit is not unexpectedly activated, causing latch-up of the ESD protection circuit; wherein the SCR circuit comprises: a P-type substrate; an N well, formed in the p-type substrate; a first P+ doped region, formed in the P-type substrate and coupled to the ground voltage; a first N+ doped region, formed in the P-type substrate, adjacent to the first P+ doped region, and coupled to the ground voltage; a second N+ doped region, formed between the P-type substrate and the N well, adjacent to the first N+ doped region, and coupled to the sixth connection terminal of the anti-latch-up circuit; a second P+ doped region, formed in the N well, adjacent to the second N+ doped region, and coupled to the I/O pad; and a third N+ doped region, formed in the N well, adjacent to the second P+ doped region, and coupled to the voltage source; wherein the anti-latch-up circuit comprises: a PMOS transistor, having a gate electrode, a source region coupled to the voltage source, and a drain region coupled to the second N+ doped region; a resistor, having a first end and a second end, respectively coupled to the gate electrode of the PMOS transistor and the ground voltage; and a capacitor, having a first contact end and a second contact end, respectively coupled to the voltage source and the gate electrode of the PMOS transistor, wherein the second N+ doped region is the third connection terminal of the SCR circuit, which receives the anti-latch-up signal so as to change a

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triggering voltage of the SCR circuit for preventing its latch-up when the to-be-protected IC is powered by the voltage source.

6. (currently amended) An electrostatic discharge (ESD) protection circuit, suitable for use on the I/O pad, the ESD protection circuit comprising: a silicon controlled rectifier (SCR) circuit, which comprises a first connection terminal, a second connection terminal, and a third connection terminal, wherein the first connection terminal and the second connection terminal are respectively connected to the I/O pad and a ground voltage, so as to discharge the electrostatic charges; and an anti-latch-up circuit, which comprises a fourth connection terminal, a fifth connection terminal, and a sixth connection terminal, respectively coupled to a voltage source, the ground voltage, and the third connection terminal of the SCR circuit, whereby when a to-be-protected IC is powered by the voltage source, an anti-latch-up signal is sent from the sixth connection terminal, so that the SCR circuit is not unexpectedly activated, causing latch-up of the ESD protection circuit; wherein the SCR circuit comprises a low-voltage triggering SCR (LVTSCR) circuit, which comprises: a P-type substrate; an N well, formed in the p-type substrate; a first P+ doped region, formed in the P-type substrate and coupled to the ground voltage; a first N+ doped region, formed in the P-type substrate, adjacent to the first P+ doped region, and coupled to the ground voltage; a second N+ doped region, formed between the P-type substrate and the N well, adjacent to the first N+ doped region, and coupled to the sixth connection terminal of the anti-latch-up circuit, wherein an additional NMOS transistor with a source/drain region and a gate is formed between the first N+ doped region and the second N+ doped region; a second P+ doped region, formed in the N well, adjacent to the second N+ doped region, and coupled to the I/O pad; and a third N+ doped region, formed in the N well, adjacent to the second P+ doped region, and coupled to the voltage source, wherein the second N+ doped region is the third connection terminal of the SCR circuit, which receives the anti-latch-up signal so as to change a triggering voltage of the SCR circuit for preventing its latch-up when the to-be-protected IC is powered by the voltage source.

7. (original) The ESD protection circuit of claim 6, wherein the anti-latch-up circuit comprises: a

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PMOS transistor, having a gate electrode, a source region coupled to the voltage source, and a drain region coupled to the second N+ doped region; a resistor, having a first end and a second end, respectively coupled to the gate electrode of the PMOS transistor and the ground voltage; and a capacitor, having a first contact end and a second contact end, respectively coupled to the voltage source and the gate electrode of the PMOS transistor, wherein the gate electrode of the additional NMOS transistor of the LVTSCR circuit is also coupled to the gate electrode of the PMOS transistor.

8. (currently amended) An electrostatic discharge (ESD) protection circuit, suitable for use on the I/O pad, the ESD protection circuit comprising: a silicon controlled rectifier (SCR) circuit, which comprises a first connection terminal, a second connection terminal, and a third connection terminal, wherein the first connection terminal and the second connection terminal are respectively connected to the I/O pad and a ground voltage, so as to discharge the electrostatic charges; and an anti-latch-up circuit, which comprises a fourth connection terminal, a fifth connection terminal, and a sixth connection terminal, respectively coupled to a voltage source, the ground voltage and the third connection terminal of the SCR circuit, whereby when a to-be-protected IC is powered by the voltage source, an anti-latch-up signal is sent from the sixth connection terminal, so that the SCR circuit is not unexpectedly activated causing latch-up of the ESD protection circuit; wherein the SCR circuit comprises: a P-type substrate; an N well, formed in the p-type substrate; a first P+ doped region, formed in the P-type substrate and coupled to the ground voltage; a first N+ doped region, formed in the P-type substrate, adjacent to the first P+ doped region, and coupled to the ground voltage; a second P+ doped region, formed between the P-type substrate and the N well, adjacent to the first N+ doped region, and coupled to the sixth connection terminal of the anti-latch-up circuit; a third P+ doped region, formed in the N well, adjacent to the second P+ doped region, and coupled to the I/O pad; and a second N+ doped region, formed in the N well, adjacent to the third P+ doped region, and coupled to the I/O pad, wherein the second N+ doped region is the third connection terminal of the SCR circuit, which receives the anti-latch-up signal so as to change a triggering voltage of the SCR circuit for preventing its latch-up when the to-be-protected IC is powered by the voltage source.

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9. (original) The ESD protection circuit of claim 8, wherein the anti-latch-up circuit comprises: a capacitor, having a first contact end and a second contact end, respectively coupled to the voltage source and the second P+ doped region; and a resistor, having a first end and a second end, respectively coupled to the second P+ doped region and the ground voltage.

10. (currently amended) The ESD protection circuit of claim 8, wherein the anti-latch-up circuit comprises: an NMOS transistor, having a gate electrode, a source region coupled to the ground voltage, and a drain region coupled to the second P+ doped region; a capacitor, having a first contact end and a second contact end, respectively coupled to the gate electrode of the PNMOS transistor and the ground voltage; and a resistor, having a first end and a second end, respectively coupled to the voltage source and the gate electrode of the PNMOS transistor.

11. (currently amended) An electrostatic discharge (ESD) protection circuit, suitable for use on the I/O pad, the ESD protection circuit comprising: a silicon controlled rectifier (SCR) circuit, which comprises a first connection terminal, a second connection terminal, and a third connection terminal, wherein the first connection terminal and the second connection terminal are respectively connected to the I/O pad and a ground voltage, so as to discharge the electrostatic charges; and an anti-latch-up circuit, which comprises a fourth connection terminal, a fifth connection terminal, and a sixth connection terminal, respectively coupled to a voltage source, the ground voltage, and the third connection terminal of the SCR circuit, whereby when a to-be-protected IC is powered by the voltage source, an anti-latch-up signal is sent from the sixth connection terminal, so that the SCR circuit is not unexpectedly activated, causing latch-up of the ESD protection circuit; wherein the SCR circuit comprises a p-type low-voltage triggering SCR (LVTSCR) circuit, which comprises: a P-type substrate; an N well, formed in the p-type substrate; a first P+ doped region, formed in the P-type substrate and coupled to the ground voltage; a first N+ doped region, formed in the P-type substrate, adjacent to the first P+ doped region, and coupled to the ground voltage; a second P+ doped region, formed between the P-type substrate and the N well, adjacent to the first N+ doped region, and coupled to the sixth

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connection terminal of the anti-latch-up circuit; a third P+ doped region, formed in the N well, adjacent to the second P+ doped region, and coupled to the I/O pad, wherein an additional PMOS transistor with a source/drain region and a gate electrode of the p-type LVTSCR circuit is formed between the second P+ doped region and the third P+ doped region; and a second N+ doped region, formed in the N well, adjacent to the third P+ doped region, and coupled to the I/O pad, wherein the second N+ doped region is the third connection terminal of the SCR circuit, which receives the anti-latch-up signal so as to change a triggering voltage of the SCR circuit for preventing its latch-up when the to-be-protected IC is powered by the voltage source.

12.(original) The ESD protection circuit of claim 11, wherein the anti-latch-up circuit comprises: an NMOS transistor, having a gate electrode, a source region coupled to the ground voltage, and a drain region coupled to the second P+ doped region; a capacitor, having a first contact end and a second contact end, respectively coupled to the gate electrode of the NMOS transistor and the ground voltage; and a resistor, having a first end and a second end, respectively coupled to the voltage source and the gate electrode of the NMOS transistor, wherein the gate electrode of the additional PMOS transistor of the p-type LVTSCR circuit is also coupled to the gate electrode of the NMOS transistor.